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REMARKS

These remarks will discuss the claim amendments, and in sections A through E will respond to the rejections of the office action of September 16, 2003.

Claim Amendments: Discussion

Claim 3 formerly depended from claim 1. Claim 1 has been cancelled and claim 3 has been amended to incorporate the subject matter of claim 1, and thus is changed in form only, not in scope.

Claims 6 and 7 have been amended to depend from claim 3 rather than from claim 1.

Claim 27 formerly depended from claim 1. Claim 1 has been cancelled and claim 27 has been amended to incorporate the subject matter of claim 1, and thus is changed in form only, not in scope.

In several rejections of the office action of September 16, 2003, the Examiner declines to give patentable weight to limitations which appear in the preamble, citing *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951). In most of these claims, patentable weight is not given to words in the preamble reciting that the device is a SONOS device or is a thin film transistor.

Applicants disagree; section 2111.02 of the MPEP, under the heading "Preamble Statements Limiting Structure," says:

> Any terminology in the preamble that limits the structure of the claimed invention must be treated as a claim limitation. See, e.g., *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1257, 9 USPQ2d 1962, 1966 (Fed. Cir. 1989).

Applicants believe limitations that imply real structure, such as the polycrystalline film of a TFT device or the ONO structure of a SONOS device, fall in this category and should be given patentable weight.

However, to clarify the claims and to address the Examiner's concern, Applicants have amended claims 9, 21-26, and 38-42 by restating a limitation of the preamble in the body of the claim. As this is merely a restatement of an existing limitation, Applicants do not consider any of these amendments to result in a change in scope.

A. Claim 7, 102(b) Rejection: Discussion

Claim 7 was rejected under 35 USC 102(b) as being anticipated by Yu et al. Claim 7 has been amended to depend from claim 3 rather than from claim 1, and thus will be discussed in section C, which addresses the rejection of claim 3.

B. Claims 6-7, 9, 12-15, 20-21, 24, 26, 27, 30-31; 102(e) Rejection: Discussion

Claims 6-7, 9, 12-15, 20-21, 24, 26, 27, and 30-31 are rejected under 35 USC 102(e) as being anticipated by Luoh et al. Claim 6 and 7 have been amended to depend from claim 3, and thus will be discussed in section C, which addresses the rejection of claim 3.

Claim 9 has been amended to recite a method for making a SONOS device, comprising providing a channel region; providing a first oxide layer on the channel region by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer, wherein the device is a SONOS device.

Referring to FIG. 2 of Luoh et al., which pictures a floating gate memory device, not a SONOS device, the Examiner asserts:

> ... Luoh discloses a method for making a SONOS device, comprising: providing a channel region (area between source and drain 19 [0019]), and providing a first oxide layer 13 on the channel region by ISSG process providing a nitride layer 14, on the first oxide layer 13, and providing a second oxide layer 16 on the nitride layer [0022].

The Examiner is correct that the region between source and drain 19 is a channel region, that oxide layer 13 is formed by an in-situ steam generation process, that layer 14 is silicon

nitride, and that layer 16 is an oxide. As evident from Fig. 2, however, oxide layer 13 is not on the channel region, but is instead on conductive layer 12. Similarly, oxide layer 16 is not on nitride layer 14, but is instead on oxynitride layer 15.

As amended, the claim also states, in both the preamble and the body, that the device is a SONOS device.

Semiconductor nonvolatile memory devices that operate by storing charge fall largely into two categories: floating gate and SONOS.

SONOS is a well-known term of art. In a SONOS device, which typically operates as a memory cell, an oxide-nitride-oxide (ONO) dielectric structure separates a gate conductor, usually of silicon, from a channel, also usually of silicon. The sequence of contiguous layers, silicon-oxide-nitride-oxide-silicon, gives the SONOS device its name. The term MONOS is also used to describe a variation on these devices, in which metal replaces silicon in the gate conductor. An example of a SONOS device appears in FIG. 1 of the present application. Oxide layer 25, formed by ISSG, is a tunnel oxide. Charge is stored in nitride layer 35.

In contrast, in a floating gate device, as in FIG. 2 of Luoh et al., charge is stored not in a nitride later, but in an electrically isolated or "floating" gate, normally of silicon. The device pictured in FIG. 1 of Luoh et al. is a floating gate device, containing floating gate 12.

An excerpt from Volume 28 of *Cx-News*, a semiconductor technical information online publication from Sony Electronics, is included in Exhibit A. In the second paragraph, this article gives an example of the terms "SONOS", "MONOS" and "floating gate" as used in the art:

> Figure 1 compares the MONOS and floating gate device structures. As can be seen in Figure 1, the MONOS name comes directly from the structure of the device. (In the US, silicon is used instead of metal, and it is called SONOS.) In

> MONOS, charge is stored in traps in the nitride layer, which is an insulator sandwiched between oxide layers, and this stored charge is used to record data.

The MONOS device shown in Figure 1 of the Sony publication and the SONOS device of Fig. 1 of the present application both show a silicon channel, and, on the channel and in contiguous contact, an oxide layer, a nitride layer, a second oxide layer, and a gate conductor. In the SONY publication the gate conductor is metal, and in the present application it may be silicon. The Sony publication notes both the metal (MONOS) and silicon (SONOS) gate conductor variations. Similarly, the present application notes that the SONOS gate conductor is "typically of polysilicon, metal, or a silicide" (paragraph [19].)

It will be seen that the floating gate device pictured in Figure 1 of the Sony publication is essentially the same as the floating gate device in Fig. 2 of Luoh et al. In both, there is a channel, then on the channel and in contiguous contact, an oxide, a polysilicon floating gate, a dielectric layer, and a control gate. The difference lies in the dielectric between the floating gate and the control gate: In the Sony publication, this dielectric layer is a single layer of silicon dioxide, while in Fig. 2 of Luoh, the dielectric comprises layers 13-16, which are oxide, nitride, oxynitride, and oxide layers respectively, all dielectrics. As noted in paragraph [0004] of the Description of Prior Art in Luoh et al.:

> In conventional stacked non-volatile semiconductor memory devices, an insulating layer for insulating a floating gate and a control gate from each other is a single layer of silicon dioxide ...

In Luoh et al., the oxide-nitride-oxynitride-oxide stack is developed to provide better insulation between the floating gate 12 and the control gate 17, as the Description of Prior Art makes clear.

The fact that the Examiner is able to identify non-contiguous layers distributed throughout a floating gate device that coincidentally correspond to the contiguous layers of a SONOS device does not make the device a SONOS device. In fact, Luoh names and teaches against even using an ONO structure (paragraphs [0005] and [0006]), the heart of a SONOS device, as insulation between the control gate 17 and the floating gate 12, arguing that the structure becomes prone to pinholes and other problems as device densities increase.

Similarly, claim 21 has been amended to recite a method for making a gate dielectric structure for a SONOS device, comprising providing silicon; providing an oxide layer of a gate dielectric structure on the silicon by in-situ steam generation, the oxide layer having a thickness of about 10 to about 200 angstroms; and annealing the oxide layer in a nitric oxide atmosphere wherein the device is a SONOS device. Like claim 9, this claim teaches, in both the preamble and the body, that the device is a SONOS device. As described, the device of Luoh et al. is a floating gate device, and therefore not a SONOS device.

The same applies to independent claims 24 and 26, both of which, as amended, recite in both the preamble and the body that the device is a SONOS device, and all thus clearly distinguish over the floating gate device of Luoh et al. Similarly, claim 27 recites, in the body of the claim, that the device is a SONOS device.

Thus Luoh et al. fails to teach each and every limitation of these claims and their dependent claims 12-15, 20, and 30-31. Applicants respectfully request that the 102(e) rejections of claims 6-7, 9, 12-15, 20-21, 24, 26, 27, and 30-31 be withdrawn.

C. Claims 3, 5, 8, 22-23, 25, 28-29, 32-34; 103(a) Rejection: Discussion

Claims 3, 5, 8, 22-23, 25, 28-29, and 32-34 are rejected under 35 USC 103(a) as being unpatentable over Luoh et al. Claim 3 recites a method for making a transistor containing a gate dielectric structure, comprising providing a gate conductor; providing a channel; and providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process, wherein the transistor is a thin film transistor.

The Examiner states:

> However, at the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ISSG dielectric structure teaching of Luoh for intended use.

No further elaboration is offered. MPEP 2143 describes the basic requirements of a *prima facie* case of obviousness:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.
>
> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.

As no attempt is made by the Examiner to identify a suggestion to modify the reference, Applicants submit that a *prima facie* case of obviousness has not been established. Applicants note that in general TFT devices have a polycrystalline rather than a monocrystalline channel region and thus are slower; in general TFT devices and non-TFT devices are used in different applications. Substitution of a thin film transistor for a transistor with its channel in a monocrystalline substrate is in no way obvious, and certainly no suggestion to make such a substitution is found in Luoh et al.

The Examiner continues:

> Furthermore, in the recitation "transistor is a thin film transistor" that has not been given patentable weight because it have been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the contradictory clause. Kropa v. Robie, 88 USPQ 478 (CCPA 1951).

The Applicant is unable to determine the applicability of *Kropa v. Robie* in this instance, in that the limitation which the Examiner declines to give patentable weight ("wherein the transistor is a thin film transistor") appears in the body of the claim, not in the preamble, in both the amended and the prior form of claim 3.

As amended, independent claim 22 includes the limitation in the body of the claim that the transistor is a thin film transistor or a SONOS transistor, and independent claims 23 and 25 include the limitation in the body of the claim that the transistor is a thin film transistor. With these limitations included in the body of the claim, no reading of *Kropa v. Robie* allows these limitations to be denied patentable weight. As has been described in this section and in section B, the device of Luoh et al. is neither a thin film transistor nor a SONOS device.

Applicants respectfully suggest that no motivation to combine the references in the manner suggested has been established for independent claims 3, 22, 23, or 25. Applicants further believe that in light of the amendments made in the present response, the limitations the Examiner proposes to deny patentable weight cannot be denied such weight. Thus Applicants request that the 103(e) rejections of these claims and their dependent claims 5-8, 29, 32, and 33 be withdrawn.

Claim 34 depends from claim 27, the rejection of which was discussed in section B.

D. Claims 36-38; 103(a) Rejection: Discussion

Claims 36-38 are rejected under 35 USC 103(a) as being unpatentable over Chang et al., US Patent No. 6,599,801 in view of Xing et al., US Publication No. 2003/0124873.

Claim 36 recites a method for making a SONOS device, comprising providing a channel region; providing a first oxide layer in contact with the channel region by an in-situ steam generation process; providing a nitride layer in contact with the first oxide layer; and providing a second oxide layer in contact with the nitride layer.

The Examiner points to the ONO (oxide-nitride-oxide) structure of the memory cell of Chang et al., in which the oxide layer in contact with the channel (between 312 and 314) is not made by an ISSG process, as in the present application. The Examiner states:

> But Chang does not disclose a method wherein the oxide layer is made by an ISSG.
>
> However, Xing reference discloses the method wherein the ONO layer, fig. 2, by ISSG, [0024] and [0025]. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the ISSG teaching of Xing to make the oxide layer as claimed, because it would have created a high quality oxide layer as taught by Xing, column [0002].

Turning to Xing et al., description starting in paragraph [0021], shortly before paragraphs [0024] and [0025] cited by the Examiner, sets out the problem:

> After deposition "as deposited" oxides are typically of poor quality in that they can contain an unacceptable amount of defects, can contain silicon dangling bonds, can contain a high hydrogen content (H) (i.e., greater than 1 atomic percent) and low density.

Xing et al. go on in paragraph [0022] to explain how to improve the poor quality of a deposited oxide by annealing the oxide "in an ambient containing atomic oxygen (O) atoms." Paragraphs [0024] and [0025], cited by the Examiner, describe creating an oxygen-containing ambient created by an ISSG process.

To summarize, claim 36 recites providing an oxide layer by an in situ steam generation process. In contrast, Xing et al. teaches depositing an oxide layer by conventional means, then annealing that oxide in an ambient containing atomic oxygen (O) atoms.

Further, the example use of the annealed oxide layer in Xing et al. teaches against its use to replace the bottom oxide layer of the ONO stack of Chang et al. The ONO stack of Chang et al. has a first oxide layer in contact with the channel. This oxide is a tunneling oxide, and it must be very thin, and very high quality. Its role is to allow tunneling during programming and erasure of the cell, and to prevent tunneling at other times. Applicants believe that Examiner is suggesting replacing this tunneling oxide with the annealed oxide of Xing et al.

In the device of Fig. 4a through 4e of Xing et al., however, the ONO structure is between a floating gate and a control gate of a floating gate memory device. The ONO structure in this device is intended to prevent electrons from crossing *at all times*. The demands on the oxide layer of this structure, which is first deposited, then annealed in an ISSG ambient, are unrelated to those of the tunneling oxide layer of Chang et al. Hence there is no motivation to combine these references in the manner described. Nor can Applicants can find any such suggestion in the Examiner's cited paragraph [0002] in Xing et al. ("because it would have created a high quality oxide layer as taught by Xing, column [0002]"):

> The present invention relates to the field of semiconductor integrated circuits and more specifically to a method of annealing a deposited silicon oxide film to improve its quality.

Further, the ISSG-*annealed* oxide of Xing et al. is not identical to an ISSG-*created* oxide as in the present invention; thus the combination of the references would not result in the present invention.

In summary, no suggestion to combine the references was provided, and the combined references fail to teach each and every element of the claim. Applicants respectfully request that the 103(a) rejection of claims 36-38 be withdrawn.

E. Claims 39-42; 103(a) Rejection: Discussion

Claims 39-42 are rejected under 35 USC 103(a) as being unpatentable over Yu et al. As amended, claims 39-42 all recite a method for making a structure, the steps including, *inter alia*, providing a channel or channel region, and providing an oxide layer of the gate dielectric structure by in situ steam generation, the oxide layer in contact with the channel.

The Examiner states that phrases in the preambles of these claims reciting SONOS device and thin film transistor limitations are not given patentable weight, again citing *Kropa v. Robie.*

As amended, all of these claims include these limitations restated *in the body of the claim.* Claim 39 recites that the device is a SONOS device; claim 40 recites that the gate dielectric structure is for a thin film transistor or a SONOS device; and claims 41 and 42 both recite the transistor is a thin film transistor.

With these limitation included in the body of the claim, Applicants believe no reading of *Kropa v. Robie* allows these limitations to be denied patentable weight. As has been described in prior sections, the device of Yu et al. is neither a thin film transistor nor a SONOS device. In summary, Yu fails to teach each and every element of the claim. Applicants respectfully request that the 103(a) rejection of claims 36-38 be withdrawn.

CONCLUSION

In view of these amendments and remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. **If any objections or rejections remain, Applicants respectfully request an interview to discuss the references.** If the Examiner has any questions, he is asked to contact the undersigned agent at (408) 869-2921.

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Pamela J. Squyres
Agent for Applicant
Reg. No. 52246

Pamela J. Squyres
Patent Agent
3230 Scott Blvd
Santa Clara, CA 95054
Tel. 408-869-2921